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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,123	08/10/2001	Afzal M. Malik	SC11773TH	4245

23125 7590 04/26/2004

FREESCALE SEMICONDUCTOR, INC.
LAW DEPARTMENT
7700 WEST PARMER LANE MD:TX32/PL02
AUSTIN, TX 78729

EXAMINER	
VO, TIM T	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 04/26/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/927,123	MALIK ET AL.	
	Examiner	Art Unit	
	Tim T. Vo	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-31,39-49 and 54-57* is/are allowed.

6)☒ Claim(s) *1-12,18-20 and 32-38* is/are rejected.

7)☒ Claim(s) *13-17 and 36* is/are objected to.

8)☒ Claim(s) *50-53* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2,3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

This application has been examined. Claims 1-57 are pending.

Election/Restrictions

1. Restriction is required under 35 U.S.C. 121 and 372.

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1.

In accordance with 37 CFR 1.499, applicant is required, in response to this action, to elect a single invention to which the claims must be restricted.

2. Group I, claims 1-49, 54-57, drawn to access arbitrating, which is classified in class 710, subclass 240.

3. Group II, claim 50-53, drawn to I/O access regulation, which is classified in class 710, subclass 36.

4. A telephone call was made to Susan Hills on February 20, 2004 to request an oral election to the above restriction requirement, Ms. Hills elected group I (claims 1-49, 54-57) with traverse.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventor ship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventor ship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(I).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless --

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1-12, 18-20 and 32-38 are rejected under 35 U.S.C. § **102(e)** as being anticipated by Rao et al. patent number 6,671,752 referred hereinafter "Rao".

As for claim 1, Rao teaches a method for prioritizing requests in a data processor having a bus interface unit, adapted to be coupled to a communications bus, which services

requests for use of the communications bus, and a plurality of resources that make requests for use of the communications bus (see figure 1, PLB Arbiter 120, processor 110, external peripheral 140 and column 3 lines 28-37, wherein the processor 110, external device 140 is connecting to an interface PLB Arbiter 120. Further, the interface PLB Arbiter 120 arbitrates the requests from all the masters, which includes the

processor 110 and external device 140 requesting for the bus 130) , a method comprising:

receiving a first request from a first resource and a second request from a second resource (see column 3 lines 28-37, wherein the first resource and second resource would be in the group of all of the masters requesting for the bus); using a threshold corresponding to one of the first resource
and the second resource to assign a priority to the first request (see figure 2 and column 5 line 64 to column 6 line 6, wherein the threshold in the FIFO 230 is being used to assign priority request for those devices requesting for the bus).

As for claims 2, 18, Rao teaches wherein using the threshold comprises using status information corresponding to the first and second resource (see figures 3A-3B and column 7 lines 50-60).

As for claim 3, Rao teaches wherein the status information is stored in a static control register (see column 3 lines 44-46).

As for claim 4, Rao teaches wherein the threshold is programmable (see column 20 lines 27-39).

As for claim 5, Rao teaches wherein the threshold is user programmable (see column 20 lines 27-39).

As for claim 6, Rao teaches wherein threshold is capable of being modified during operation of the data processor (see column 20 lines 27-36).

As for claims 7, 19-20 and 33-35, Rao teaches wherein the threshold is adaptively modified by a performance monitor, in response to evaluating performance of the data

processor (see column 17 lines 38-40).

As for claim 8, Rao teaches wherein the first resource comprises a write buffer which makes requests for use of the communications bus for transferring information to a memory (see column 6 lines 49-61).

As for claim 9, Rao teaches wherein the second resource comprises an instruction prefetch buffer which makes requests for use of the communications bus for receiving instructions from the memory (see column 6 lines 49-61).

As for claim 10, Rao teaches wherein the data processor has a cache, adapted to be coupled to the communications bus, and the second resource includes a push buffer which make requests for use of the communications bus for transferring information to the memory (see figure 1, data cache 114).

As for claim 11, Rao teaches wherein the first resource includes an instruction prefetch buffer and the second resource includes a push buffer (column 6 lines 49-61).

As for claims 12, 32 and 37, Rao teaches a data processor comprising: a central processing unit (see figure 1, processor core 110); a first requesting resource coupled to the central processing unit (see figure 1, wherein other resources such as other processor core 110, external 140, memory controller 150 are connecting to the bus 130 requesting to own the bus 130, and adapted to request use of a communications bus for transmitting or receiving data (see figures 1-2 and column 6 lines 49-61); a second

requesting resource coupled to the central processing unit (see figure 1, wherein second requesting resources are other processor core 110, external 140, memory controller 150, and adapted to request use of the communications bus for transmitting or receiving data (see column 6 lines 49-61); and a bus interface unit coupled to the central processing unit (see figure 1, arbiter 120, the first requesting resource, and the second requesting resource, and adapted to be coupled to the communications bus (see figure 1, processor core 110, peripheral controller 140, memory controller 150 are coupling to the bus 130), the bus interface unit further comprising: a priority controller coupled to receive a first request from the first requesting resource and a second request from the second requesting resource (see figure 1, arbiter 120), and to assign a priority to each of the first and second request based on a threshold corresponding to one of the first requesting resource and the second requesting resource (see figure 2 and column 5 line 64 to column 6 line 6, wherein the threshold in the FIFO 230 is being used to assign priority request for those devices requesting for the bus).

Allowable Subject Matter

7. Claims 21-31, 39-49 and 54-57 are allowable over the prior of records.

8. Claims 13-17, 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Examiner's Statement of Reasons for Allowance

The following is an Examiner's statement of reasons for the indication of allowable subject matter: Claims 21, 39, 47, 54 and 56 are allowable over the prior art of record

because the Examiner found neither prior art cited in its entirety, nor based on the prior art, found any motivation to combine any of the said prior arts. As for claim 21, prior art fails to teach priority rules specification circuitry, wherein the priority rules specification circuitry comprises a first programmable threshold register which stores a first threshold corresponding to the write buffer and current priority resolution circuitry coupled to the priority rules specification circuitry which receives memory access requests from the cache and the write buffer and which prioritizes the memory access requests based at least one the first threshold. As for claims 39, 47 and 56, prior arts fails to teach comparing number of valid entries with the write buffer with a write buffer threshold to obtain a first comparison result and comparing a number of valid entries within the instruction prefetch buffer with an instruction prefetch buffer threshold to obtain a second comparison result. As for claim 54, prior art fails to teach comparing number of entries within the prefetch buffer with a prefetch buffer threshold and in response to comparing the number of entries, selectively affecting a priority of the change of flow instruction fetch request to a request from the prefetch buffer for use of the communication bus.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim T. Vo whose telephone number is 703-308-5862. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tim T. Vo
Primary Examiner
Art Unit 2112

4/20/04